WHAT IS CLAIMED IS:

1. A system for determining whether arcing is present in an electrical circuit in response to a sensor signal corresponding to current in said circuit, said system comprising:

a circuit for analyzing said sensor signal to determine the presence of broadband noise in a predetermined range of frequencies, and producing a corresponding output signal; and

a controller for processing said sensor signal and said output signal to determine current peaks and current rise time and to determine, using said current peaks and rise times and the presence of broadband noise, whether an arcing fault is present in said circuit, by comparing data corresponding to said current peaks and rise times and broadband noise with preselected data indicative of an arcing fault;

wherein said circuit for analyzing and said controller are integrated onto a single application specific integrated circuit chip (ASIC).

2. The system of claim 1 wherein the controller includes a plurality of counters and increments said plurality of counters in response to said sensor signal and said output signal, and periodically determines whether an arcing fault is present by monitoring said plurality of counters and comparing counts in said counters with one or more preselected counts indicative of an arcing fault.

3. The system of claim 2 wherein said counters are implemented in software.

4. The system of claim 1 wherein said integrated chip further includes an onboard voltage regulator for providing regulated DC voltage supplies for all of the analog and digital circuits on said integrated circuit chip.

5. The system of claim 1 wherein said controller comprises a microprocessor.

6. The system of claim 1 wherein said circuit for analyzing includes at least two bandpass filters having different passbands, and a set of comparators for monitoring

outputs of said bandpass filters, said comparators having outputs which change state when a predetermined threshhold is exceeded.

7. The system of claim 6 wherein said circuit further includes at least one counter which is incremented in response to components of high frequency in the pass bands of at least two of said bandpass filters which are simultaneously present.

8. The system of claim 7 wherein said bandpass filters are switched capacitor bandpass filters, and further including at least one AND gate synchronized with said switched capacitor bandpass filters for ANDing said comparator output to said counter.

9. The system of claim 1 wherein said circuit comprises a plurality of operational amplifiers, and wherein said controller further is operative for coupling each of said operational amplifiers with an analog reference voltage, reading an offset voltage of said operational amplifier and storing the value of said offset voltage in a memory, and thereafter subtracting said offset voltage values from measured signal values for each of said operational amplifiers.

10. The system of claim 1 wherein said controller produces a trip signal in response to a determination that an arcing fault is present, and further latches said trip signal until reception of a reset signal.

11. The system of claim 10 wherein said controller powers down the other circuits on said integrated circuit chip when said trip signal is given, using stored energy to maintain the trip signal.

12. The system of claim 6 wherein said integrated circuit chip further includes a test signal buffer which acts as a current source for driving a test winding at a center frequency of each of the bandpass filters.

13. The system of claim 1 wherein said integrated circuit chip includes three channels, a muliplexer for selecting each channel, and a single channel analog-to-digital

converter for receiving and converting a signal on the channel selected by said multiplexer.

14. The system of claim 1 wherein said integrated circuit chip further includes circuits for forming, together with an external sensor, a dormant oscillator neutral detection system for detecting a grounded neutral.

15. The system of claim 14 wherein said circuits for forming a dormant oscillator neutral detection system includes a first amplifier for comparing a ground fault input signal from said external sensor to a reference, and a second amplifer coupled in series with said first amplifier for providing sufficient loop gain to put the dormant oscillator into oscillation in response to a grounded neutral condition.

16. A method for determining whether arcing is present in an electrical circuit in response to a sensor signal corresponding to current in said circuit, said system comprising, on a single application specific integrated circuit chip:

analyzing said sensor signal to determine the presence of broadband noise in a predetermined range of frequencies, and producing a corresponding output signal; and

processing said sensor signal and said output signal to determine current peaks and rise times and to determine, using said current peaks and rise times and the presence of broadband noise, whether an arcing fault is present in said circuit, by comparing data corresponding to said current peaks and rise times and broadband noise with preselected data indicative of an arcing fault.

17. The method of claim 16 including incrementing a plurality of counters in response to said sensor signal and said output signal, and periodically determining whether an arcing fault is present by monitoring said plurality of counters and comparing counts in said counters with one or more preselected counts indicative of an arcing fault.

18. The method of claim 17 wherein said counters are implemented in software.

19. The method of claim 16 further including providing regulated DC voltage supplies for all of the analog and digital circuits on said integrated circuit chip, using an onboard voltage regulator.

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20. The method of claim 16 wherein said processing is performed by a microprocessor.

21. The method of claim 16 wherein said analyzing includes passing said sensor signal through at least two bandpass filters having different passbands, and monitoring outputs of said bandpass filters, with comparators having outputs which change state when a predetermined threshhold is exceeded.

22. The method of claim 21 further including incrementing at least one counter in response to the simultaneous presence of components of high frequency in the pass bands of at least two of said bandpass filters.

23. The method of claim 21 and further including synchronizing at least one AND gate with said bandpass filters for ANDing said comparator outputs.

24. The method of claim 16 further including coupling each of a plurality of operational amplifiers with an analog reference voltage, reading an offset voltage of said operational amplifier and storing the value of said offset voltage in a memory, and thereafter subtracting said offset voltage values from measured signal values for each of said operational amplifier.

25. The method of claim 16 further including producing a trip signal in response to determining an arcing fault is present, and latching said trip signal until reception of a reset signal.

26. The method of claim 25 including powering down circuits on said integrated circuit chip when said trip signal is given, using stored energy to maintain the trip signal.

27. The method of claim 21 further including driving a test winding at a center frequency of each of the bandpass filters.

28. A system for determining whether arcing is present in an electrical circuit in response to a sensor signal corresponding to current in said circuit, said system comprising, on a single application specific integrated circuit chip:

means for analyzing said sensor signal to determine the presence of broadband noise in a predetermined range of frequencies, and producing a corresponding output signal; and

means for processing said sensor signal and said output signal to determine current peaks and current rise times and to determine, using said current peaks, said current rise times and the presence of broadband noise, whether an arcing fault is present in said circuit, by comparing data corresponding to said current peaks and rise times and broadband noise with preselected data indicative of an arcing fault.

29. The system of claim 28 including means for incrementing a plurality of counters in response to said sensor signal and said output signal, and means for periodically determining whether an arcing fault is present, including means for monitoring said plurality of counters and means for comparing counts in said counters with one or more preselected counts indicative of an arcing fault.

30. The system of claim 29 wherein means for said counters are implemented in software.

31. The system of claim 28 further including means for providing regulated DC voltage supplies for all of the analog and digital circuits on said integrated circuit chip, using an onboard voltage regulator.

32. The system of claim 28 wherein said means for processing comprises a microprocessor.

33. The system of claim 28 wherein said means for analyzing includes passing said sensor signal through at least two bandpass filters having different passbands, and monitoring outputs of said bandpass filters, with comparators having outputs which change state when a predetermined threshhold is exceeded.

34. The system of claim 33 further including means for incrementing at least one counter in response to the simultaneous presence of components of high frequency in the pass bands of at least two of said bandpass filters.

35. The system of claim 33 and further including means for synchronizing at least one AND gate with said bandpass filters, for ANDing said comparator outputs.

36. The system of claim 28 further including means for coupling each of a plurality of operational amplifiers with an analog reference voltage, means for reading an offset voltage of said operational amplifier, means for storing the value of said offset voltage in a memory, and means for subtracting said offset voltage values from measured signal values for each of said operational amplifier.

37. The system of claim 28 further including means for producing a trip signal in response to determining an arcing fault is present, and latching said trip signal until reception of a reset signal.

38. The system of claim 37 including means for powering down circuits on said integrated circuit chip when said trip signal is given, using stored energy to maintain the trip signal.

39. The system of claim 33 further including means for driving a test winding at a center frequency at each of the bandpass filters.

40. The method of claim 24 and further including periodically repeating said coupling, reading and storing to update said offset voltage values.

41. The system of claim 1 wherein said integrated circuit chip comprises a processor responsive to an externally generated test mode signal for causing said test signal buffer to generate a signal for driving said test winding.

42. The method of claim 27 wherein said driving is performed in response to an externally generated test mode signal.

43. The system of claim 39 and further including means responsive to a test mode signal for triggering said means for driving.

44. The system of claim 1 and further including, on said ASIC, a port for bi-directional exchange of data between said ASIC and an external processor.

45. The method of claim 27 and further including bi-directionally exchanging data between said ASIC and an external processor.

46. The system of claim 39 and further including means for bi-directionally exchanging data between said ASIC and an external processor.